

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claim 1 (previously presented): An interface circuit conforming to multiple bus standards, comprising:

a first interface circuit conforming to a first bus standard;

a second interface circuit conforming to a second bus standard; and

a common set of pins coupled to the first interface circuit and the second interface circuit and a host computer bus, the common set of pins being user selectable to communicate with the host computer bus in accordance with either the first bus standard or the second bus standard.

Claim 2 (previously presented): The interface circuit of claim 1, wherein the common set of pins is configured to transmit and receive data conforming to either a PCI bus standard or a PCMCIA bus standard.

Claim 3 (previously presented): The interface circuit of claim 1, wherein the first bus standard comprises a PCI standard.

Claim 4 (previously presented): The interface circuit of claim 3, wherein the second bus standard comprises a PCMCIA standard.

Claim 5 (original): The interface circuit of claim 1, further comprising a multi-voltage input output buffer coupled to each pin.

Claim 6 (original): The interface circuit of claim 1, further comprising an internal bus coupled to the first and second interface circuit.

Claim 7 (previously presented): The interface circuit of claim 6, wherein the first interface circuit is configured to format signals on the internal bus to signals compliant with the first bus standard.

Claim 8 (currently amended): An interface circuit comprising: ~~The interface circuit of claim 7, wherein~~

a first interface circuit conforming to a first bus standard;

a second interface circuit conforming to a second bus standard;

a common set of pins coupled to the first interface circuit and the second interface circuit and a host computer bus, the common set of pins being user selectable to communicate with the host computer bus in accordance with either the first bus standard or the second bus standard;  
and

an internal bus coupled to the first and second interface circuit, wherein the first interface circuit is configured to format signals on the internal bus to signals compliant with the first bus standard and the second interface circuit is configured to format signals on the internal bus to signals compliant with the second bus standard.

Claim 9 (original): The interface circuit of claim 1, further comprising a first power supply to supply voltage swings in accordance with the first bus standard.

Claim 10 (currently amended): ~~The interface circuit of claim 9, further comprising:~~ An interface circuit

a first interface circuit conforming to a first bus standard;

a second interface circuit conforming to a second bus standard;

a common set of pins coupled to the first interface circuit and the second interface circuit and a host computer bus, the common set of pins being user selectable to communicate with the host computer bus in accordance with either the first bus standard or the second bus standard;

a first power supply to supply voltage swings in accordance with the first bus standard;  
and

a second power supply to supply voltage swings in accordance with the second bus standard.

Claims 11-20 (cancel)